Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1-14. (cancelled)

15. (new) An integrated circuit, comprising:

a substrate; and

a bias circuit, disposed on the substrate, for establishing a plurality of bias voltages from an input current supplied to an input terminal, the bias circuit comprising

an input stage adapted to establish a first bias voltage at the input terminal in response to the input current,

a current stage adapted to produce a bias current and a main mirror current each proportional to the input current in response to the first bias voltage and a second bias voltage,

a feedback stage adapted to produce a feedback current proportional to the input current in response to the bias current and the main mirror current, and

a reference bias stage adapted to establish the second bias voltage in response to the feedback current from the feedback stage, whereby the first and second bias voltages track the input current over variations in at least one of process, temperature and power supply voltage.

16. (new) The integrated circuit of claim 15, wherein the feedback stage of the bias circuit comprises:

a reference voltage stage adapted to establish third and fourth bias voltages in response to the bias current and the main mirror current; and

a current source adapted to produce the feedback current in response to the third and fourth bias voltages.

17. (new) The integrated circuit of claim 16, wherein the reference voltage stage of the bias circuit comprises:

a bias stage adapted to establish the third bias voltage in response to the bias current; and

a reference stage adapted to establish the fourth bias voltage in response to the main mirror current and the third bias voltage.

18. (new) The integrated circuit of claim 16, wherein the input stage and the reference bias stage are each constructed using transistors of a first type such that the first and second bias voltages are suitable for biasing current sources constructed using transistors of the first type, and wherein the reference voltage stage is constructed using transistors of a second type complementary to the first type such that the third and fourth bias voltages produced thereby are suitable for biasing current sources constructed using transistors of the second type.

19. (new) The integrated circuit of claim 16, wherein the reference voltage stage is constructed using p-type Metal Oxide Semiconductor (PMOS) transistors such that the third and fourth bias voltages established thereby are suitable for biasing one or more current sources constructed using PMOS transistors.

20. (new) The integrated circuit of claim 15, wherein the input stage and the reference bias stage are each constructed using n-type Metal Oxide Semiconductor (NMOS) transistors such that the first and second bias voltages established thereby are suitable for biasing one or more current sources constructed using NMOS transistors.

21. (new) The integrated circuit of claim 15, wherein the input stage includes an input transistor configured as a diode and connected between the input terminal and a power supply rail of the circuit, thereby establishing a gate-source voltage and a drain-source voltage of the input transistor corresponding to the input current, and wherein the current stage includes a bias current stage having a first transistor adapted to produce the bias current, the first transistor having a gate connected to the input terminal to establish a gate-source voltage of the first transistor equal to a gate-source voltage of the input transistor, and a second transistor connected to the first transistor in a cascode configuration and adapted to maintain a source-drain voltage of the first transistor equal to the source-drain voltage of the input transistor in response to the second bias voltage such that the bias current produced by the first transistor is proportional to the input current.

22. (new) The integrated circuit of claim 15, wherein the input stage includes an input transistor configured as a diode and connected between the input terminal and a power supply rail of the circuit, thereby establishing a gate-source voltage and a drain-source voltage of the input transistor corresponding to the input current, and wherein the current stage includes a main mirror current stage having a first transistor adapted to produce the main mirror current, the first transistor having a gate connected to the input terminal to establish a gate-source voltage of the first transistor equal to a gate-source voltage of the input transistor, and a second transistor connected to the first transistor in a cascode configuration and adapted to maintain a source-drain voltage of the first transistor equal to the source-drain voltage of the input transistor in response to the second bias voltage such that the main mirror current produced by the first transistor is proportional to the input current.

23. (new) The integrated circuit of claim 15, further comprising:

an input resistor connected between a first power supply rail at a first power supply voltage and the input terminal of the bias circuit, to set a value of the input current supplied to the input terminal, wherein the input stage is connected between the input terminal and a second power supply rail at a second power supply voltage, the input stage being adapted to provide a voltage drop between the input terminal and the second power supply rail approximating a voltage drop across a single diode, whereby the input stage minimizes sensitivity of the circuit to fluctuations in the first power supply voltage.

24. (new) The integrated circuit of claim 23, wherein the input stage is a transistor configured as a diode connected between the input terminal and the second power supply rail.

25. (new) The integrated circuit of claim 15, wherein the bias circuit further comprises:

a start-up stage adapted to provide a trickle-current to the reference bias stage to force the bias circuit into a stable operating condition.

26. (new) The integrated circuit of claim 25, wherein the start-up stage is adapted to reduce the trickle current from an initial current value to a final current value in response to a rise in the second bias voltage established by the reference bias stage.

27. (new) The integrated circuit of claim 25, wherein the start-up stage includes one of a resistor connected between a terminal common to both the feedback stage and the reference bias stage and a power supply rail, and a plurality of transistors having their respective source-drain current paths connected in series with one another, the series connected source-drain paths being connected between a power supply rail and a terminal common to both the feedback stage and the reference bias stage.

28. (new) The integrated circuit of claim 15, wherein the bias circuit further comprises:

a shut-down stage adapted to selectively enable and disable the supply of the input current to the input terminal so as to selectively enable and disable an operation of the bias circuit, respectively.

29. (new) The integrated circuit of claim 28, wherein the shut-down stage includes a transistor having a source-drain path connected to the input terminal and being adapted to shunt the input current away from the input terminal so as to disable the operation of the circuit in response to a control voltage applied to a control electrode of the transistor.

30. (new) A circuit for establishing a plurality of bias voltages suitable for biasing current sources from an input current, comprising:

means for supplying an input current;

means for establishing a first bias voltage in response to the input current;

means for producing a bias current proportional to the input current in response to the first bias voltage and a second bias voltage;

means for producing a main mirror current proportional to the input current in response to the first bias voltage and the second bias voltage;

means for producing a feedback current proportional to the input current in response to the bias current and the main mirror current; and

means for establishing the second bias voltage in response to the feedback current, whereby the first and second bias voltages track the input current over variations

in at least one of a temperature of the circuit and a power supply voltage provided to the circuit.

31. (new) The circuit of claim 30, wherein third and fourth bias voltages are established in response to the bias current and the main mirror current, and wherein the feedback current is produced in response to the third and fourth bias voltages.

32. (new) The circuit of claim 30, further comprising:

means for supplying a trickle current to establish a stable operating condition of the circuit.

33. (new) The circuit of claim 32, further comprising:

means for reducing the trickle current from an initial current value to a final current value in response to a rise in the second bias voltage indicative of the stable operating condition.

34. (new) A method of establishing a plurality of bias voltages suitable for biasing current sources from an input current supplied to a bias circuit, comprising:

(a) establishing a first bias voltage in response to an input current;

(b) producing a bias current proportional to the input current in response to the first bias voltage and a second bias voltage;

(c) producing a main mirror current proportional to the input current in response to the first bias voltage and the second bias voltage;

(d) producing a feedback current proportional to the input current in response to the bias current and the main mirror current; and

(e) establishing the second bias voltage in response to the feedback current of step (d), whereby the first and second bias voltages track the input current over variations in at least one of a temperature of the bias circuit and a power supply voltage provided to the bias circuit.